AF301

QSFP (Quad Small Form-Factor Pluggable) FMC Board

Applications
- Wideband data communication
- Data storage interface

Features
- One QSFP (Quad Small Form-Factor Pluggable) interface
- Supports QSFP copper or optical transceivers up to 6.25 Gbps/lane
- On board low jitter reference clock generator
- VITA 57 FMC form factor
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores

Overview
The AF301 is part of ApisSys' range of modular IOs solutions based on the VITA 57, FPGA Mezzanine Card standard.

The AF301, quad channel optical link FMC mezzanine, provides customers with one QSFP (Quad Small Form-Factor Pluggable) transceiver supporting up to four serial links (optical or copper) at up to 6.25 Gbps per link.

The AF301 supports serial communication protocols such as GigE, SATA, SRI0, XAUI or Aurora up to 6.25 Gbps, as well as PCIe x4 gen1 and gen 2.

The AF301 provides an on board, user programmable, low jitter clock generator supporting reference clocks as required for PCIe, SATA, SRI0, Fiber Channel, Aurora, Gbit Ethernet or XAUI protocols.

The AF301 is fully supported on ApisSys 3U VPX FPGA processing engines, making it ideally suited for data communication, Electronic Warfare, Ultra Wideband Radar Receivers or LiDAR applications.
Quad Small Form-Factor Pluggable Transceiver

The AF301 is a wideband data communication interface board supporting one Quad Small Form-Factor Pluggable (QSFP) transceiver.

The AF301 supports optical QSFP transceivers for communication at up to 40 Gbps over distances up to 10 km.

The AF301 supports copper QSFP transceivers for communication at up to 40 Gbps over distances up to a few meters.

Clocks

The AF301 provides an on-board, user programmable, low jitter clock generator generating clock references as required for the high speed serial links (Xilinx Virtex® 6 GTX). The clock frequency can be selected among the following:

- 100 MHz, supporting PCIe gen 1
- 125 MHz, supporting PCIe gen 1, GigE, Aurora and SRIO 1.25 and 2.5 Gbps
- 150 MHz, supporting SATA
- 156.25 MHz, supporting XAUI, SRIO and Aurora 3.125 Gbps
- 250 MHz, supporting PCIe gen 2
- 312.5 MHz, supporting Aurora 5 and 6.25 Gbps

FMC interface

The AF301 features a VITA 57 – FMC (FPGA Mezzanine Card) compliant slot.

The AF301 supports the Multi-gigabit differential pairs DP0 to DP3 for the QSFP interface.

The AF301 requires the use of HB00 to HB06 for board configuration and supervision.

Firmware

The AF301 comes with a firmware package which includes VHDL cores allowing for control and communication with all AF301 hardware resources.

A base design is provided demonstrating the use of the AF301. It gives users a starting point for firmware development.

The AF301 firmware package is supported on the Xilinx ISE® 13 design suite and later versions.

The AF301 firmware package has been fully validated on the AV103 and other ApisSys FMC carrier products.

Software

The AF301 is delivered with software drivers for Windows XP and 7, and Linux, compatible with the AV103 and other ApisSys FMC carrier products.

An application example is provided as source code.

Ruggedization

The AF301 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC3.
Specifications

QSFP cage and connector
- Compliant with QSFP standard
- 38-contact QSFP connector

Reference Clock
- 100 MHz, supported protocols:
  - PCIe gen 1
- 125 MHz, supported protocols:
  - PCIe gen 1
  - GigE
  - Aurora 1.25 and 2.5 Gbps
  - Aurora 1.25 and 2.5 Gbps
- 150 MHz, supported protocols:
  - SATA
- 156.25 MHz, supported protocols:
  - XAUI 3.125 Gbps
  - SRIO 3.125 Gbps
  - Aurora 3.125 Gbps
- 250 MHz, supported protocols:
  - PCIe gen 2
- 312.25 MHz, supported protocols:
  - Aurora 5 and 6.25 Gbps

FMC interface
- HPC:
  - LA(0:33): not used
  - HA(0:23): not used
  - HB(0:6): LVCMOS 2.5V

Software support
- Software Drivers:
  - Windows XP and 7
  - Linux
- Application example:
  - Windows and Linux

Power Mgmt
- DC/DC

FMC HPC

Clock synthesizer

QSFP

QSFP cage and connector

GTX x4

I2C - CTRL

Fiber or copper

Power dissipation
- +12V: 0 A (0W)
- +3.3V: 0.2 A (0.6W) no transceiver
- VADJ (2.5V): 0.1 A (0.3W)
- +3.3VAUX: <0.1 A

Ruggedization
- As per VITA 47:
  - Air cooled: EAC4 and EAC6
  - Conduction cooled: ECC3

Firmware support
- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx ISE 14 and later

Weight
- Air cooled: 50g
- Conduction cooled: 55g
## Ruggedization levels

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>0°C to +55°C (1) (8 CFM airflow at sea level)</td>
<td>-40 to +70°C (1) (8 CFM airflow at sea level)</td>
<td>-40°C to +70°C (Card Edge)</td>
<td>-40°C to +85°C (Card Edge)</td>
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<tr>
<td>Non Operating Temperature</td>
<td>-40°C to +85°C</td>
<td>-50°C to +100°C</td>
<td>-50°C to +100°C</td>
<td>-55°C to +105°C</td>
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<tr>
<td>Operating Vibration</td>
<td>5Hz - 100Hz +3 dB/octave</td>
<td>5Hz - 100Hz +3 dB/octave</td>
<td>5Hz - 100Hz +3 dB/octave</td>
<td>5Hz - 100Hz +3 dB/octave</td>
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<tr>
<td>Random Vibration</td>
<td>100Hz - 1kHz = 0.04 g²/Hz</td>
<td>100Hz - 1kHz = 0.04 g²/Hz</td>
<td>100Hz - 1kHz = 0.1 g²/Hz</td>
<td>100Hz - 1kHz = 0.1 g²/Hz</td>
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<tr>
<td>1kHz - 2kHz = 6 dB/octave</td>
<td>1kHz - 2kHz = 6 dB/octave</td>
<td>1kHz - 2kHz = 6 dB/octave</td>
<td>1kHz - 2kHz = 6 dB/octave</td>
<td>1kHz - 2kHz = 6 dB/octave</td>
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<tr>
<td>Operating Shock</td>
<td>20g, 11 millisecond, half-sine</td>
<td>20g, 11 millisecond, half-sine</td>
<td>40g, 11 millisecond, half-sine</td>
<td>40g, 11 millisecond, half-sine</td>
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<tr>
<td>Operating Relative Humidity</td>
<td>0% to 95% non-condensing</td>
<td>0% to 95% non-condensing</td>
<td>0% to 95% non-condensing</td>
<td>0% to 95% non-condensing</td>
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<tr>
<td>Operating Altitude</td>
<td>@ 0 to 10,000 ft with adequate airflow</td>
<td>@ 0 to 30,000 ft with adequate airflow</td>
<td>@ 0 to 30,000 ft with adequate airflow</td>
<td>@ 0 to 60,000 ft</td>
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<tr>
<td>Conformal Coating</td>
<td>No</td>
<td>Optional (default acrylic 1B31)</td>
<td>Yes (default acrylic 1B31)</td>
<td>Yes (default acrylic 1B31)</td>
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## Ordering information

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<thead>
<tr>
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<th>A</th>
<th>F</th>
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<tbody>
<tr>
<td>Ruggedization level</td>
<td>Air Standard</td>
<td>AS</td>
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<tr>
<td>Air Rugged</td>
<td>AR</td>
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<tr>
<td>Conduction Standard</td>
<td>CS</td>
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<tr>
<td>Conduction Rugged</td>
<td>CR</td>
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